AMENDMENTS TO THE CLAIMS

Claim 1. (Cancelled)

2. (Currently Amended) The method of claim [[1]] 9 wherein a path from the adjacent programmable interconnect point to one of the input and the output is generated by an auto-route tool.

3. (Original) The method of claim 2 wherein the path excludes the line segment.

4. (Currently Amended) The method of claim [[1]] 9 wherein the first adjacent programmable interconnect point is on the line segment.

5. (Currently Amended) The method of claim [[1]] 9 wherein the switch matrix is incorporated in a programmable logic device.

6. (Currently Amended) The method of claim [[1]] 9 wherein the second test vector is the same as the first test vector.

7. (Currently Amended) The method of claim [[1]] 9 wherein the step of generating the second route is performed prior to the step of applying the first test vector.

8. (Original) The method of claim 7 wherein the first route and the second route are stored in a route directory.

9. (Previously Presented) A method of locating a fault on a failed line segment of a switch matrix comprising:

generating a first route between an input of the switch matrix and an output of the switch matrix through a first programmable interconnect point on the line segment and

through a first adjacent programmable interconnect point;

configuring the first route in the switch matrix;

applying a first test vector at the input;

measuring first test data at the output;

generating a second route between the input and the output through the first programmable interconnect point on the line segment and through a second adjacent programmable interconnect point;

configuring the second route in the switch matrix;

applying a second test vector at the input;

measuring second test data at the output; and

comparing the first test data and the second test data against a layout schematic of a programmable logic device so as to locate the fault on the failed line segment.

10. (Previously Presented) A method of isolating a fault on a line segment of a switch matrix comprising:

generating a first route between an input of the switch matrix and an output of the switch matrix through a first programmable interconnect point on the line segment and through a first adjacent programmable interconnect point;

configuring the first route in the switch matrix;

applying a first test vector at the input, the first test vector comprising a first series of first digital test values followed by a second series of second digital test values followed by a third series of the first digital test values;

measuring first test data at the output;

storing the first test data and at least a portion of the first route;

generating a second route between the input and the output through the first programmable interconnect point on the line segment and through a second adjacent programmable interconnect point;

configuring the second route in the switch matrix;

applying a second test vector at the input;

measuring second test data at the output;

storing the second test data and at least a portion of the second route.

11. (Original) The method of claim 10 wherein there are at least three first digital test values in the first series.

12. (Original) The method of claim 11 wherein there are at least three second digital test values in the second series.

13. (Original) The method of claim 1 wherein the line segment includes at least four programmable interconnect points.

14. (Currently Amended) A method of isolating a fault on a line segment of a switch matrix comprising:

(a) identifying original programmable interconnect points ("PIPs") in the line segment;

(b) looking up adjacent PIPs in a PIPs database, each of the adjacent PIPs being adjacent to at least one original PIP;

(c) generating a first route through a first port of the switch matrix to an Nth original PIP where N is an integer;

(d) adding a second route from the Nth original PIP to an Mth adjacent PIP where M is a second integer;

(e) adding a third route from the adjacent PIP to a second port of the switch matrix;

(f) storing a route including the first route, second route, and third route in a route directory;

(g) repeating steps (d), (e) and (f) for all adjacent PIPs adjacent to the original PIP;

(h) repeating steps (c), (d), (e), (f) and (g) for all original PIPs;

(i) configuring the route in the switch matrix;

(j) applying a test vector at an input of the route;

(k) reading test data at an output of the route;

(l) storing the test data; ~~and~~

(m) repeating steps (i), (j), (k) and (l) for all routes in the route directory; and if a fault is detected,

(n) correlating the fault with a particular location of the switch matrix.

15. (Currently Amended) A system of isolating a fault on a line segment of a switch matrix comprising:

means for identifying original programmable interconnect points on the line segment;

means for identifying programmable interconnect points adjacent to each of the original programmable interconnect points;

means for generating routes between an input of the line segment and an output of the line segment through each of the original programmable interconnect points and through each of the programmable interconnect points adjacent to each of the original programmable interconnect points; [[and]]

means for testing the routes; and

means for correlating the fault with a particular location on the line segment.

16. (Currently Amended) A system for fault isolation on a line segment in an integrated circuit (IC) having at least one programmable interconnection, the system comprising:

a database having the at least one programmable interconnection in the IC;

a processor coupled to the database and to a memory having a test path generation software module, the test path generation software module comprising:

code for identifying original programmable interconnections on the line segment having a fault;

code for identifying programmable interconnections adjacent to the original programmable interconnect points;

code for generating routes between an input of the line segment and an output of the line segment through the original programmable interconnections and through the programmable interconnections adjacent to the original programmable interconnections; and

a tester coupled to the processor and the IC having the line segment, the tester for testing the line segment using the generated routes; and

a failure analysis software module stored in the memory and configured to receive test results related to the line segment from the tester and to perform fault isolation analysis on the received test results to correlate a fault on the line segment with a particular location of the IC.

Claim 17. (Cancelled)

18. (Previously Presented) The system of claim 16 further comprising:

a test input file comprising the generated routes and test vectors for the generated routes, the file sent to the tester by the processor;

a test results file comprising the test results on the line segment from the tester.

19. (Previously Presented) The system of claim 18 wherein information used by the tester from the test input file is modified based on feedback from the failure analysis software module.

20. (Original) The system of claim 16 wherein the database further comprises the original programmable interconnections and the programmable interconnections adjacent to the original programmable interconnections.

21. (Original) The system of claim 16 wherein the IC comprises a programmable logic device (PLD).

22. (Original) The system of claim 21 wherein the database further comprises all the original programmable interconnections on the PLD.

23. (Currently Amended) A method for fault isolation on a line segment in an integrated circuit (IC) having at least one programmable interconnection, the method comprising:

identifying an original programmable interconnection point on the line segment having a fault;

identifying an output programmable interconnection point adjacent to the original programmable interconnection point; [[and]]

generating a route between an input of the line segment and an output of the line segment through the original programmable interconnection point and through the output programmable interconnection point; and

correlating the fault with a particular location on the integrated circuit (IC).

24. (Original) The method of claim 23 further comprising:

identifying an input programmable interconnection point adjacent to the original programmable interconnection point; and

generating another route between an input of the line segment and an output of the line segment through the original programmable interconnection point and through the input programmable interconnection point.

25. (Currently Amended) The method of claim 24 further comprising:

testing the generated route on the line segment in the integrated circuit (IC) to produce a test result on whether a generated route passes or fails a test; ~~and~~

~~analyzing~~, wherein the step of correlating the fault includes comparing the test result against a layout schematic of the integrated circuit (IC) to determine a location of the fault on the line segment.